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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,529	02/08/2002	Michael Richard Betker	7-1-3-12-5	2912

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EXAMINER	
RAMPURIA, SATISH	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,529	BETKER ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the Amendment received on Oct. 03, 2005.

2. Claims pending in the application: 1-12.

Response to Arguments

3. Applicant's arguments with respect to claim 1 have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

(i) Alverson fails to teach or suggest these (Alverson describes the replacement of a specified instruction within the executable code with a breakpoint instruction. Obviously, this type of replacement step must occur before the breakpoint can be executed. In claim 1, on the other hand, the steps following the words "after the breakpoint is executed" explicitly occur after a breakpoint instruction is encountered within the executable code) elements of claim 1. Moreover, Dunlap does not correct this fundamental deficiency in Alverson. Accordingly, not all elements of claim 1 are taught or suggested by the proposed reference combination.

(ii) Applicants suggest that this portion (See Remarks page 4) of Dunlap, nor any other portion for that matter, fails at least to describe the portion of claim 1 wherein the use-once indicator "is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache." Accordingly, this element of claim 1 is also not taught or suggested by the Alverson-Dunlap reference combination.

Examiner's response:

(i) In response to Applicants arguments, Alverson disclose debugging techniques for the target system. Alverson discloses replacement of a specified instruction within the nub thread execution routine (see Fig. 5) where the replacement is done dynamically after the thread execution routine is invoked (See Fig. 5 and col. 14-15) execution executable. Further, as claimed in claim 1, step 3 that breakpoint is inserted before the execution and obviously if the breakpoint is inserted it will get executed to perform an action. Inserting a breakpoint is well known to one skill in the art. Therefore, the rejection is proper and maintained herein.

(ii) In response to Applicants arguments, In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, It is noted that the rejection clearly points out where the combination of Alverson and Dunlap teach the claimed features and why it would have been obvious to combine their teachings. Dunlap does disclose the COF flag that indicates that a COF, such as a branch instruction (conditional or unconditional) has been taken. The Instruction pointer stores the next instruction address provided by

functional unit for use as required by instruction decode/dispatch logic (or cache control logic to clear a validity indicator). COF address register also stores the next instruction address, which is serially shifted out of microprocessor starting when the COF flag is active (See FIG. 2-3 and related discussion). Thus, the COF flag is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache. Therefore, the rejection is proper and maintained herein.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,848,097 Alverson et al. (hereinafter called Alverson) in view of US Patent No. 6,615,368 to Dunlap (hereinafter called Dunlap).

Per claim 1:

Alverson disclose:

- A method of implementing a software breakpoint in a multiprocessor system having a plurality of processors each coupled to a main memory (col. 7, lines 36-37 "present invention provide various techniques for debugging targets"), each of the processors having an instruction cache associated therewith (See Fig.1 and related discussion), the method comprising the steps of:
- retrieving an instruction, for which the breakpoint is to be inserted, from a corresponding instruction address in the main memory (col. 7, lines 39-40 "implementing breakpoints using out-of-line instruction");
- inserting a breakpoint code at the instruction address in main memory (See Fig. 5 and related discussion); and
- after the breakpoint code is executed by a given one of the processors, storing the retrieved instruction in the corresponding instruction cache for that processor (col. 15, lines 45-50 "determine whether the request is a request from the debugger to create a breakpoint at a specified instruction within the executable code of the target. If so, the routine continues to step 515 to allocate memory for the instruction group to be

generated") and such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory (col. 15, lines 51-54 "The routine continues at step 520 where the generated instruction group is installed in the allocated memory, and information about the created group is stored in an accessible location").

Alverson does not explicitly disclose setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor, wherein the use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache.

However, Dunlap discloses in an analogous computer system setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor (col. 3, lines 27-29 "executing the debugging instruction enables a selected flag in the data processor"), wherein the use-once indicator, when set for the instruction as stored in the instruction cache (col. 6, lines 42-44 "COF address... detects the COF flag and loads the next instruction address... to external devices"), is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache (col. 6, lines 46-48 "the next instruction address is stored... sent to decode/dispatch logic... uses it to fetch the new instruction from the new branch").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of setting a flag for the software breakpoint in the memory as taught by Dunlap into the method of implementing software breakpoint in a shared memory system as taught by Alverson. The modification would be obvious because of one of ordinary skill in the art would be motivated to have flags in a software breakpoint method to provide an optimize technique for debugging as suggested by Dunlap (col. 1, lines 51-61).

Per claim 2:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the instruction cache includes a plurality of sets of instruction information (col. 16, lines 10-13 "nub will itself execute one or more instructions for which a breakpoint has been set"), each corresponding to a particular instruction, a given one of the sets of instruction information comprising the validity indicator, the use-once indicator, an instruction tag, and instruction data (col. 16, lines 24-40 "determine if the received request is a directive from the debugger indicating to begin execution of one or more target threads or to resume execution of one or more halted target threads. If so, the routine continues at step 545 to notify the target threads to begin or continue execution as directed").

Per claim 3:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the instruction address comprises an instruction tag, an index and a block offset.

The limitation recited in this claim are similar to those recited in claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Per claim 4:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the cache control logic is operative to compare portions of the instruction address to corresponding portions of instruction information as stored in the instruction cache and checks the validity indicator in determining if there is a hit or a miss between the instruction address and the instruction information as stored in the instruction cache (See Fig. 5 and related discussion).

Per claim 5:

The rejection of claim 1 is incorporated, and further, Alverson does not explicitly disclose wherein the use-once bit when set, being operative via the cache control logic to clear the validity indicator associated with the instruction as stored in the instruction cache after a single fetch of the instruction from the instruction cache, thereby automatically causes a miss between the instruction address and the instruction as stored in the instruction cache when the given processor attempts to retrieve the instruction from the instruction cache subsequent to the single fetch.

However, Dunlap discloses in an analogous computer system wherein the use-once bit when set, being operative via the cache control logic to clear the validity indicator associated

with the instruction as stored in the instruction cache after a single fetch of the instruction from the instruction cache (col. 6, lines 40-45 "functional units determines that a change of flow (COF)... flag is set... detects the active COF flag and loads the next instruction address... to external devices"), thereby automatically causes a miss between the instruction address and the instruction as stored in the instruction cache when the given processor attempts to retrieve the instruction from the instruction cache subsequent to the single fetch (col. 6, lines 46-50 "next instruction address is stored... sent to instruction decode/dispatch logic... uses fetch instruction from new branch... processing continues").

The feature of using use-once bit to clear the validity indicator would be obvious for the reasons set forth in the rejection of claim 1.

Per claim 6:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the use-once indicator associated with the instruction comprises a single bit stored in a given set of the instruction cache. The limitation recited in this claim are similar to those recited in claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Per claim 7:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the validity indicator associated with the instruction comprises a single bit stored in a given set of the instruction cache (See Fig. 4A and Fig. 4B and related discussion).

Per claim 8:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the instruction for which the breakpoint is to be inserted comprises an instruction having a noncacheable attribute associated therewith. The limitation recited in this claim are similar to those recited in claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Per claim 9:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein at least a subset of the retrieving, inserting, storing and setting steps are implemented under the control of a debugger which interfaces with the multiprocessor system. The limitation recited in this claim are similar to those recited in claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Per claim 10:

The rejection of claim 1 is incorporated, and further, Alverson disclose:

- wherein the breakpoint code inserted at the instruction address in main memory comprises a debug opcode. The limitation recited in this claim are similar to those recited

in claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Claims 11 and 12 are the system and computer program product claims respectively corresponding to method claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2191
12/27/2005

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